DEVELOPMENT OF A NEW LINAC RF PEAK DETECTOR UNIT AT THE AUSTRALIAN SYNCHROTRON

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Abstract

An RF peak detector unit forms part of the LINAC at the Australian Synchrotron (AS). The system captures a maximum of 12 pulsed RF signals from six bi-directional couplers to measure forward and reverse powerlevels. This unit has been successfully replaced with an I/Q demodulator, which also provides phase information to ease tuning and to diagnose instabilities. The new system now has 16 channels with enhanced performance. Data acquisition has also been upgraded to a high accuracy PCI board with EPICS interface for consistency with our control system.

INTRODUCTION

The AS 100 MeV 3 GHz LINAC structure is made of a 90 keV thermionic electron gun (GUN), a 500 MHz subharmonic prebuncher unit (SPB) -, preliminimary buncher (PBU), final buncher (FBU) and two accelerator structures. The structures are powered by two 35 MW pulsed klystrons, and transmitted across the SF6 pressurised WR284 waveguide RF distribution system. The low level electronics include two pulsed 400W S band amplifiers to drive the klystrons, and two UHF amplifiers for the GUN and SPB. All of which are manually adjustable in phase and amplitude [1]. Details of the LINAC layout are shown in Figure 1.

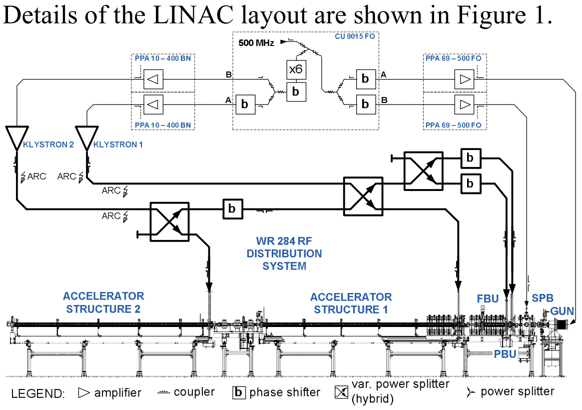


Figure 1 LINAC layout

The AS has been operating in top-up mode since May 2012, and reinjects a bunchtrain every few minutes to maintain 200 mA in the 3 GeV Storage Ring. Several upgrades of the LINAC have been necessary since operations started in 2007 in order to improve reliability. The major upgrades for the LINAC include: the timing system [2], waveguide extension [3] and the phase monitoring system described in this paper.

ORIGINAL DESIGN

The original RF peak detector is based on an AD8362 50 Hz to 3.8 GHz 65 dB true rms-responding power detector. A variable gain amplifier (VGA) enables a measuring range of 65 dB, and the output is directly converted to a logarithmic scale of 1 V per decade. The overall system design takes advantage of a frequency range between 0.5 and 3 GHz, a useful dynamic range of 40 dB up to +5 dBm and an amplified output of 0.2 V/dB up to 10 V. The following sample and hold circuit (S&H) captures pulses of ≥ 2.5 microseconds (µs) at a repetition rate of up to 100 Hz. Additionally a potentiometer adjustable high speed comparator supervises the powerlevel and outputs a latched digital signal for power exceeded interlock. The output is potential free and can handle 24V with a response time in the order of 20 µs. A peak detector module processes one RF forward or reverse signal only, and is built into a cassette. Six modules can fit into a 19” crate 420 mm deep. It requires two crates to process six bi-directional couplers.

The peak detector was integrated into the LINAC control system with limited data acquisition. A Siemens PLC processes the analogue forward power signals with a soft interlock power exceeded and the digital reverse power exceeded signals. The response time cannot provide an immediate interruption during a pulse, but disables the next shot in case of an alarm until manually reset. All RF input signals were additionally filtered with a bandpass (BP) and the displayed power resolution is 1 MW indicating possible noise issues with this design.

NEW SYSTEM

The idea of LINAC phase monitoring stems from an earlier I/Q demodulator system developed by the Swiss Light source [4], but using instead the advanced 400 MHz to 6 GHz quadrature demodulator ADL-5380. This approach simplified the design to fit two channels on a single Euro board, each channel measuring I and Q with a 5380 but also amplitude with an 8362 for power exceeded interlocks in order replace the old peak detector unit. Up to eight modules can be plugged into the 19 inch RF shielded rack 320 mm deep and an extra slot is allocated for a future module to provide a fast fault memory with a nanosecond switch to interrupt the RF. The back half of the crate hosts a 500 MHz to 3 GHz frequency multiplier and signal distribution to provide a 0 dBm reference signal to all boards. The designed backplane keeps the wiring tidy. It provides two 50 pin plugs to connect all signals directly to the ADC PCI card via system cables, or the digital signals can be redirected to a 20 pin plug and connected to a PLC for safety reasons. The heavy low loss microwave cables from the LINAC are connected to an adjacent N type patch panel, followed by attenuators for level adjustment before being connected to the SMA RF inputs. Additionally, external filterers can be added here if required. All wiring from the patch panel to the modules is made of semi rigid cable to ensure phase stability. Details of the system layout are shown in Figure 2 and a flow diagram of a module in Figure 3.

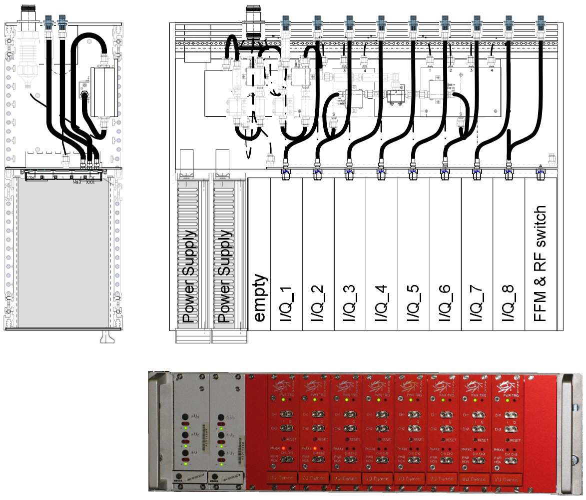


Figure 2 LINAC phase monitoring system layout

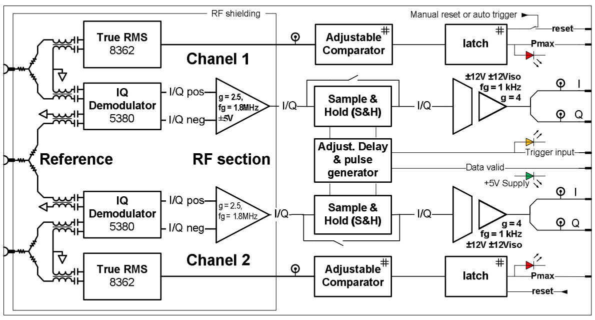


Figure 3 LINAC phase monitoring module flow diagram

A single euro board covers a frequency range of 400 MHz to 3 GHz mixing directly to baseband and provides > 40 dB dynamic range. The minimum measurable pulsewidth is ≥ 1.5 µs including rise time. A two stage S&H circuit holds I and Q up to one second for possible asynchron data acquisition. The repetition rate is 10 Hz but can easily be increased up to a few 100 Hz when bypassing the second S&H stage or fully bypassed for CW measurements. Good I/Q demodulation accuracy is achieved with amplitude and phase balances of ~0.07 dB and ~0.7 °, respectively at 3 GHz. The 5380 buffered baseband outputs are capable of driving a 2 V p-p differential signal into 200 Ω, but it has been limited to ~1 V p-p in our design. This approach did minimise intermodulation products when mixing down to an intermediate frequency (IF) instead of baseband, and it provides also extra head room to the maximum input power level of 25 dBm without damage to the system. The RF signal levels are approximately 11 dBm at 500 MHz and 15 dBm at 3 GHz to reach the maximum output level of ± 10 V. A 1.8 MHz lowpass (LP) filter after the 5380 reduces further intermodulation products and noise. The rise time remains, despite filtering at ~ 200 ns or ~0.35/BW. A second 1 kHz LP filters the outputs extra for the ADC. The differential dc offsets are compensated by software or optionally can also be adjusted manually with extra space allocated on the printed circuit board (PCB) for potentiometers. The trigger signal for the S&H circuit can be delayed by up to 5.6 µs and is adjustable in 100 ns steps with an 8 bit dipswitch on the board. This feature is also useful for testing without the need of a delay generator. Two 12 bit dipswitches set the trip level for power exceeded at a resolution of ~ 0.02 dB. Front panel monitoring outputs for I, Q and power, status LED's for board supply, trigger and power exceeded are useful debugging supports plus on board test pins. Special effort was put into a low noise design and good EMC practices. Key design features for this approach include: low emission P/S's from Kniel, isolation to mains and all outputs, short RF microstrip lines close to the connectors, and building all modules into cassettes - or optionally to cover the RF section only. Additionally, the data valid signal is delayed by 50 milliseconds to mask transients caused during a sampling cycle.

A National Instrument NI PCI-6224 16-Bit, 250 KS/s provides the data acquisition for the 32 analogue I and Q output signals, 16 digital power exceeded signals, data valid and reset. The 6224 fits into the IOC of the LINAC control system and is linked with two commercially available system cables type SHC88-EMM. The evaluation of the 6224 was based on existing EPICS drivers and exceeded our minimum requirements.

A Graphical User Interface (GUI) has been prepared to calibrate the measurements and to calculate power and phase where:

(i) $\mathrm{I} = \mathrm{I}_{meas} - \mathrm{I}_{offset};\ \mathrm{Q} = \mathrm{Q}_{meas} - \mathrm{Q}_{offset}$,

(ii) $\mathrm{Phase} = \mathrm{atan2}(\mathrm{Q}, \mathrm{I})$,

(iii) $\mathrm{P} = 0.001\ \mathrm{W} * 10^{\frac{\mathrm{dB}_{PBC+IQ+DC+cb+atten}}{10}}$,

(iv) $dB_{PCB} = dBm_{Pin} - dB_{IQ}$, gain module

(v) dBm_{Pin} , input power in dBm.

(vi) $dB_{IQ} = 10 * \log_{10}(I^2 + Q^2)$,

(vii) dB_{DC}, coupling factor directional couplers (DC),

(viii) dB_{CB}, cable losses from DC to N type patch panel,

(ix) dB_{atten}, losses from N type patch panel to backplane incl. attenuators, filters, and cables.

All dB values are manually entered into the GUI while zero set buttons are provided to calibrate I and Q to compensate the DC offsets, or to set the phase to zero degrees.

MEASUREMENTS WITH THE NEWSYSTEM

We measured a useful dynamic range of >40 dB and a demodulation accuracy of better than 0.1 dB and 1 degree respectively. Errors caused by imbalance, offsets or crosstalk were negligible. Figure 4 shows the test results, including the uncertainty in the measurements caused by the trombone and the RF peak detector meter. Note, the converted ln functions into $\log_{10}$ becomes $y[dBm] = 20\log_{10}(x[mV]) - (60 + g_{PCB})$, and the theoretical factor before ln is $20\log_{10}(e) = 8.686$.

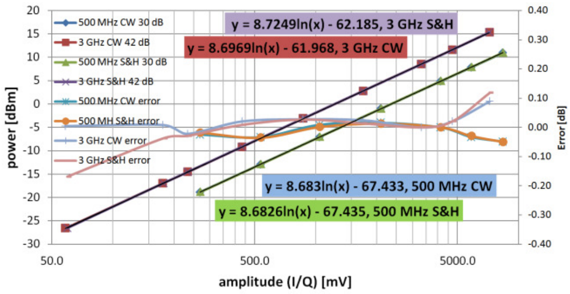
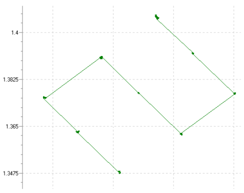
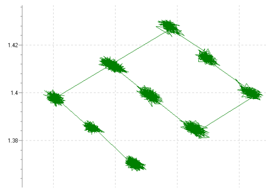


Figure 4 dynamic range

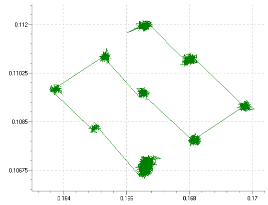
The measured noise figures were excellent and achieved a resolution of 0.1 degrees and 0.02 dB respectively; and still remarkably 1 deg and 0.2 dB at -32 dB in pulsed mode. These measurements are illustrated in the following pictures after 15 minutes warm up time in order to achieve thermal stability.



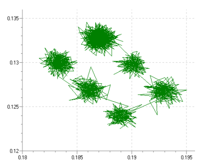
Input: 3 GHz, CW, 2.4 dBm
steps:0.1 dB/0.5 ps (0.54 deg)
scale: 17.5 mV/div



Input: 3 GHz, SH, 2.4 dBm
steps:0.1dB 0.5ps (0.54 deg)
scale:20 mV/div



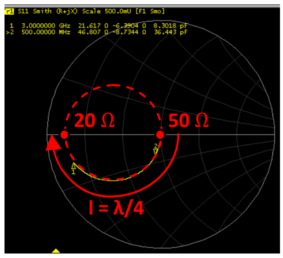
Input: 3 GHz, CW, -17dBm
steps: 0.1 dB/0.5 ps (0.54 deg)
scale:1.75/2.00 mV/div



Input: 3 GHz SH -17dBm
steps: 0.2dB 1ps (1.08deg)
scale: 5 mV/div

Figure 5 resolution

Both gains for CW and pulsed mode are equal without the need for adjustment. This is also very beneficial to ease calibration. The difference in gain between 500 MHz and 3 GHz is caused by the 5380, input balun and VSWR. The gain has to be measured for all boards due to a variation of up to 2.5 dB. The measured characteristic impedance of the microstrip lines were 32 Ω and a VSWR of ~ 1:3 at 3 GHz and < 1:1.2 at 500 MHz. This happened despite careful calculation and using high quality RF PCB material type RO4350. Two extra test microstrip lines were included into the design of the PCB for this test to illuminate any faulty manufacturing. Figure 6 illustrates the λ/4 measurement with a Smith chart and measuring S11.



$$Z_o = \sqrt{Z_{in} * Z_L}$$

$$= \sqrt{20 * 50} = 31.6\ \Omega$$

Figure 6 characteristic impedance of a microstrip line

Material costs for one complete system are less than AU$ 20,000, including assembly but they can easily be reduced to suit a tighter budget. Possibilities are shielding only the RF section instead of PCB cassettes, integration of the frequency multiplier and distribution onto the backplane or letting components out such as the LEMO debugging outputs, or no pluggable SMB connectors. Optionally the isolation amplifiers do not have to be populated should the ADC already provide isolation. This would also minimise the accumulated DC offsets.

CONCLUSION

The new in-house designed LINAC RF peak detector unit has been operating successfully since May 2012. The compact system provides excellent performance, EMC, thermal stability using convectional cooling only and will minimise maintenance without the need to retune elements on the boards. The system has already proven to be a great diagnostic tool for trouble shooting. The next upgrades will be a FFM and nanosecond switch module and possibly the same upgrade for the Booster RF system. Future development of a soft Low Level Electronics system is also likely, to automatically readjust slow drifts in phase and amplitude.

ACKNOWLEDGEMENTS

Special thanks to all of those involved in this project, and also to the ESLS-RF Workshop, which is continually a source of inspiration and support for the AS.

REFERENCES

[1] Ch. Piel et al, “commissioning of the Australian synchrotron injector RF systems” EPAC 2006, Edinburgh, Scotland

[2] E. van Garderen et al, “Upgrade of the Timing System at the Australian Synchrotron”, DIPAC09, Basel.

[3]Rohan Dowd et al, “Linac Waveguide Upgrade at the Australian SynchrotronLight Source”, IPAC2011, San Sebastián, Spain

[4]M Gaspar et al, “phase shifter and IQ demodulator, ESLS-RF/2003 Karlsruhe.