

Australian
Synchrotron

Turning bright ideas into brilliant outcomes

DEVELOPMENT OF RF PEAK DETECTOR AND PHASE MONITORING UNIT AT THE AUSTRALIAN SYNCHROTRON

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by



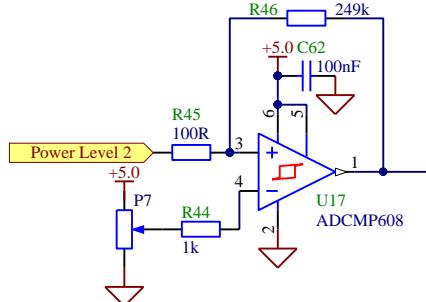
Australian Government



THE NEED



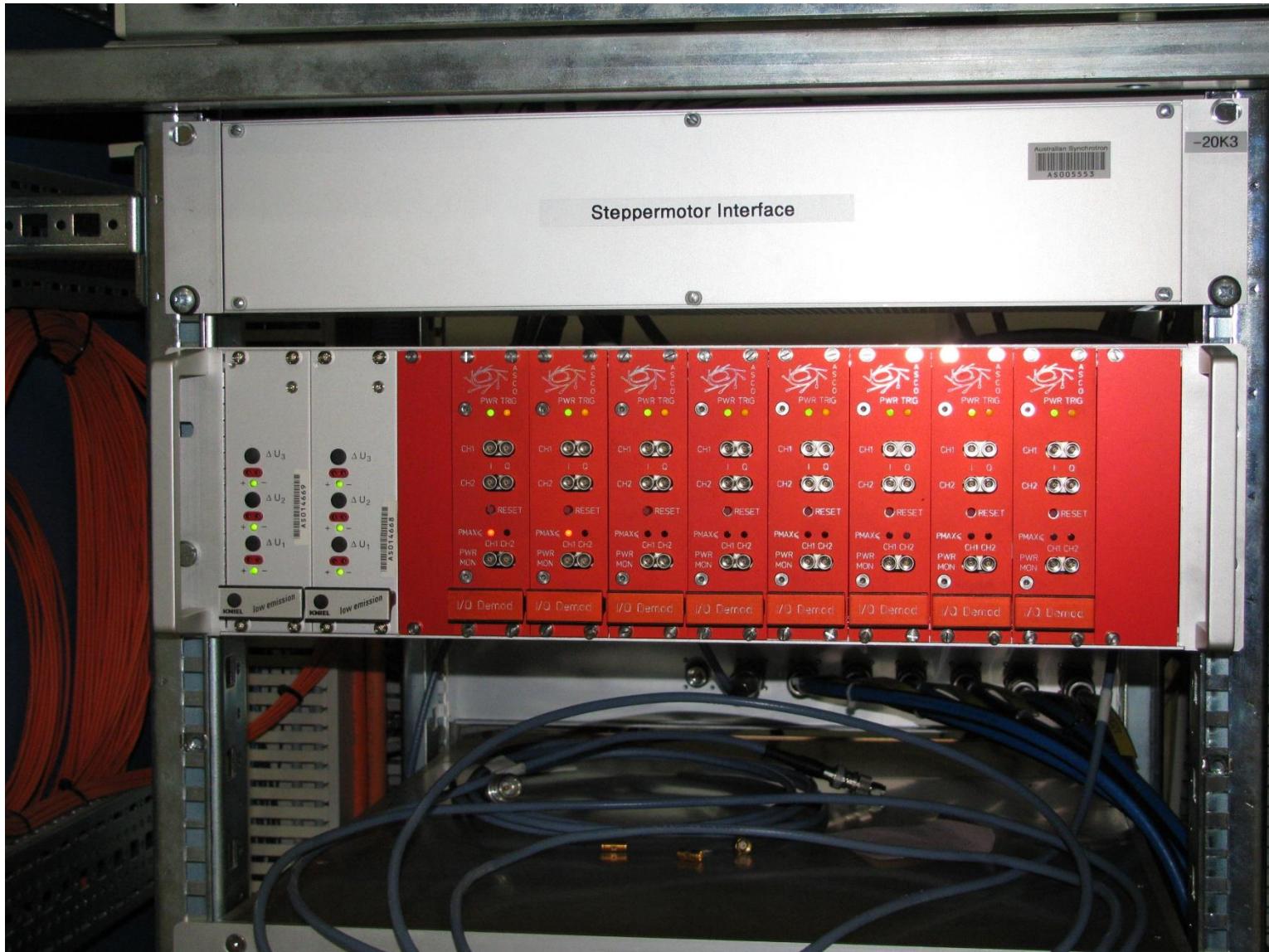
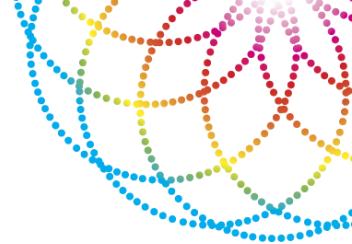
- Existing system had insufficient Peak Detector accuracy
- Existing Peak Detector was also manifesting stability and/or noise issues
- Availability of spares - customized solution
- We needed phase monitoring system to improve diagnostic
- Possibility of saving space



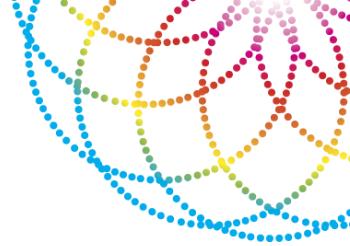
Power comparator – very, very bad example of reference voltage



WHAT WE BUILD?



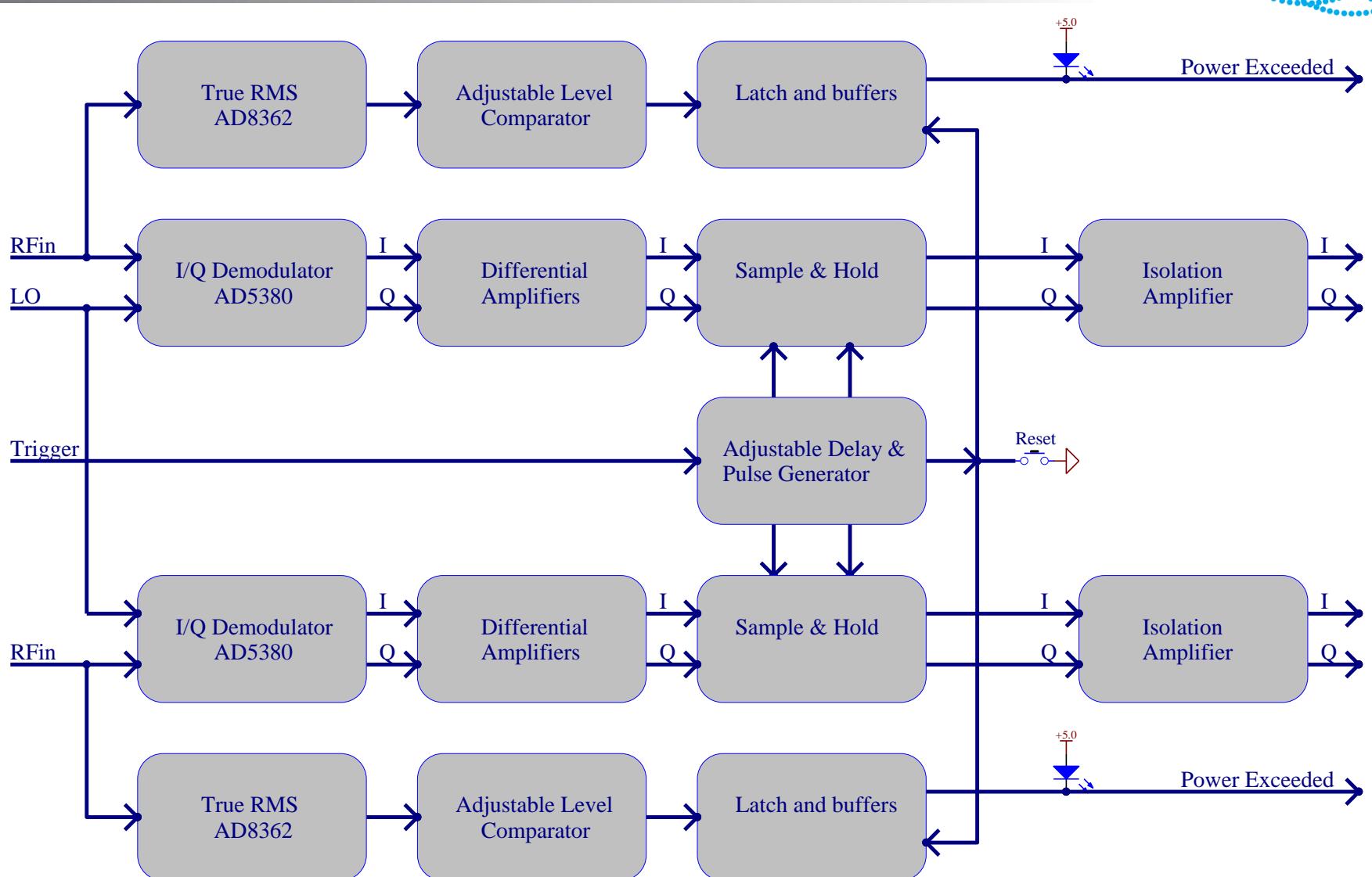
SPECIFICATION



- Isolation from mains and all auxiliary voltages derived from mains
- System should avoid earth loops
- Should be capable of continuous waveform (CW) or synchronised pulsed measurements
- Measurements between pulsed and CW mode should vary no more than 0.1dB
- The system shall be calibrated at nominal power and provide a linearity of better than ± 0.3 dB for a dynamic range of > 30 dB
- Phase accuracy should be better than two degrees and phase resolution better than half a degree at nominal power.
- The minimum frequency range for the system is from the MO reference frequency up to six times the MO frequency.
- All phase measurements are relative to the reference signals.
- The maximum system input power level shall be:

500 MHz	11 dBm and
3 GHz	15 dBm

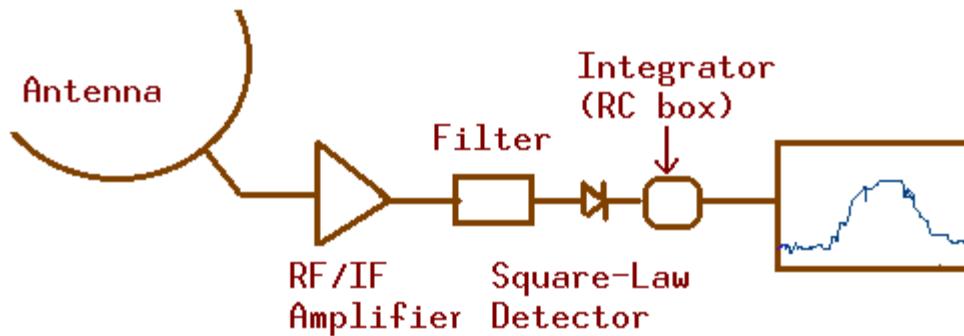
PROPOSAL OF SYSTEM ARCHITECTURE



PEAK DETECTOR - POWER METER



Square Law Detector - output DC is voltage proportional to the input power

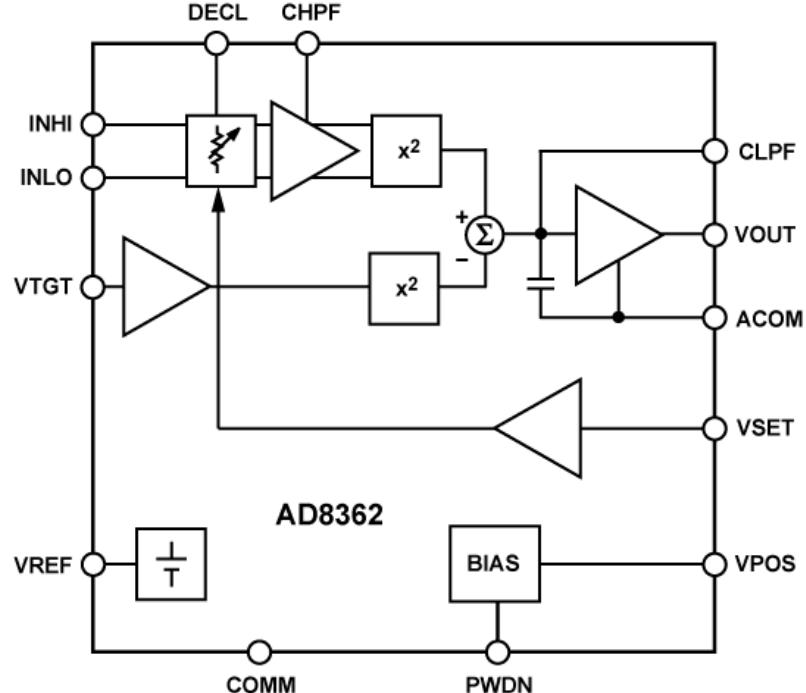


PEAK DETECTOR - POWER METER

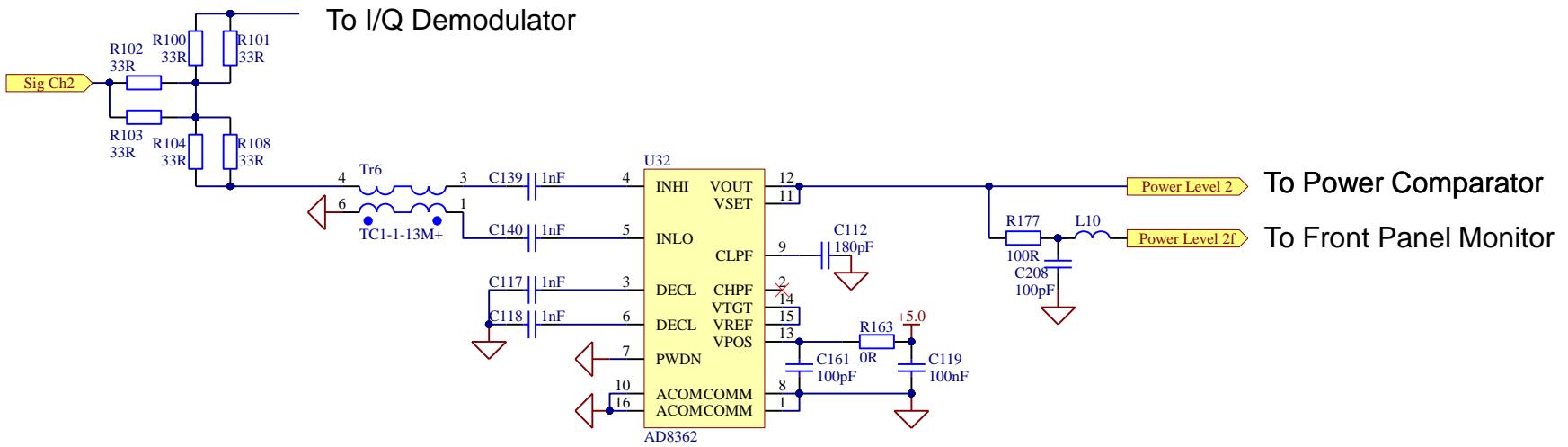


Key Features of AD8362 (square-law detector):

- Complete fully calibrated measurement/control system
- Accurate rms-to-dc conversion from 50 Hz to 3.8 GHz
- Input dynamic range of >65 dB: -52 dBm to +8 dBm in 50 Ω
- Waveform and modulation independent, such as GSM/CDMA/TDMA
- Linear-in-decibels output, scaled 50 mV/dB, Law conformance error of 0.5 dB
- All functions temperature and supply stable
- Operates from 4.5 V to 5.5 V at 24 mA
- Power-down capability to 1.3 mW

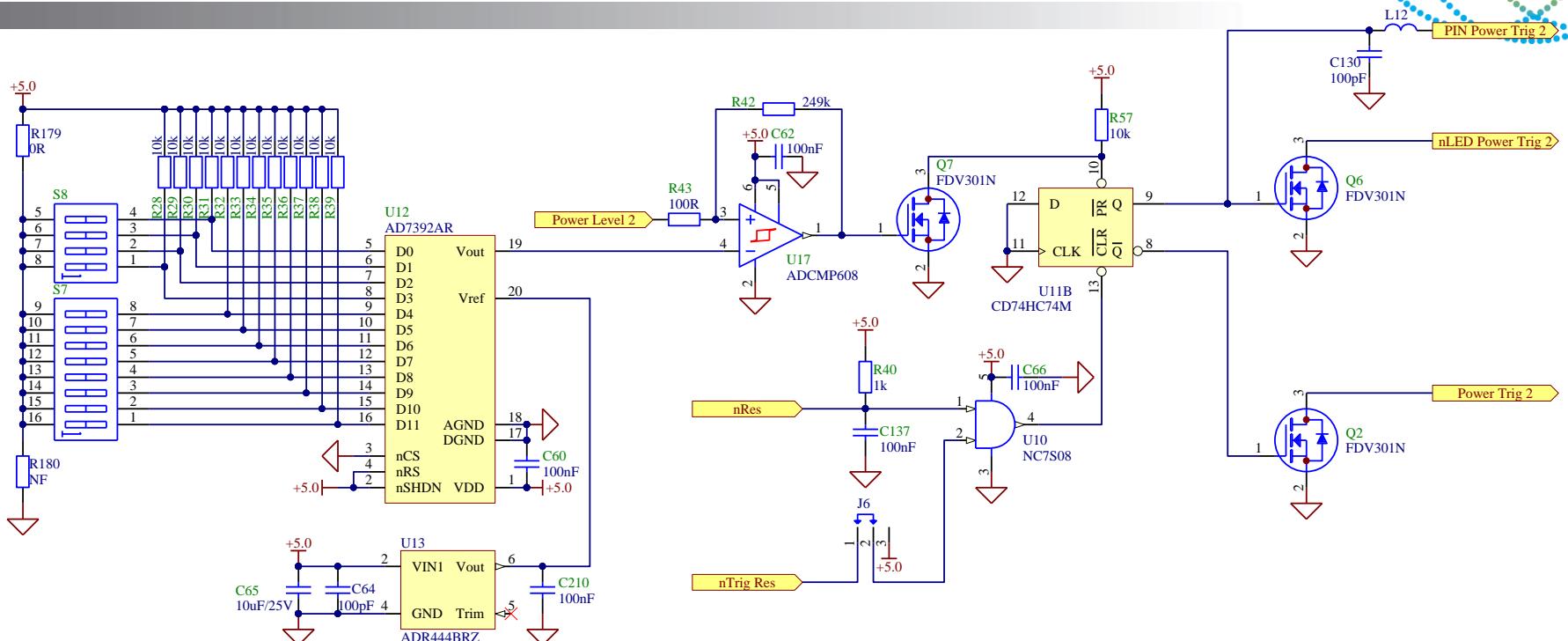


PEAK DETECTOR - POWER METER



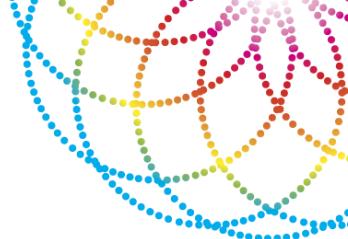
- CLPF capacitor sets corner frequency of the filter. We had to experimentally select the value to avoid overshoots creating false Power Exceeded trips.
- Additional Front Panel Output allow us to monitor power envelope of the signal.
- R177, L10 and C208 are output and EMC protection components.
- Resistive splitter provides signal to Power Meter and I/Q Demodulator

PEAK DETECTOR - COMPARATOR

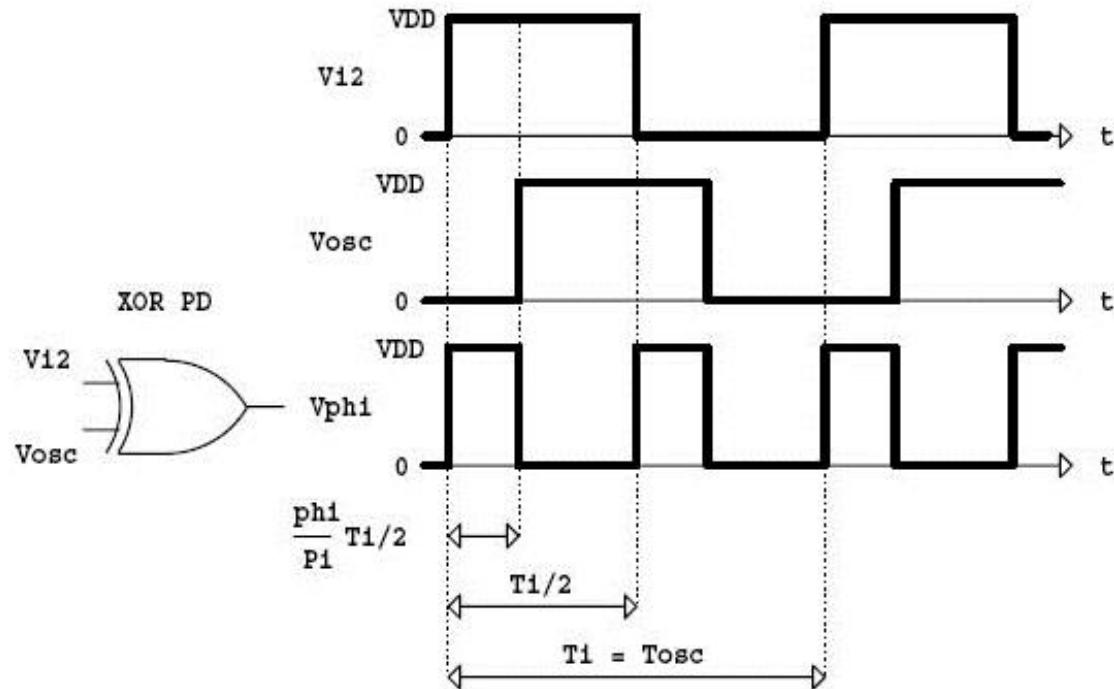


- Fast comparator with additional hysteresis
- U12 Digital to Analog converter – 12 bits ($2^{12}=4096$)
- U13 – Reference Voltage – 4.096V
- U11 – Power exceeded latch.
- U10 – Few reset options.

I/Q DEMODULATOR



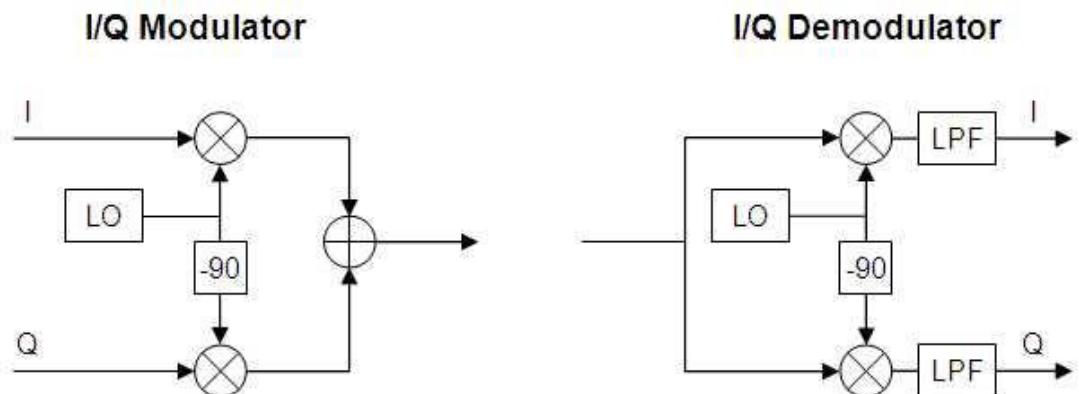
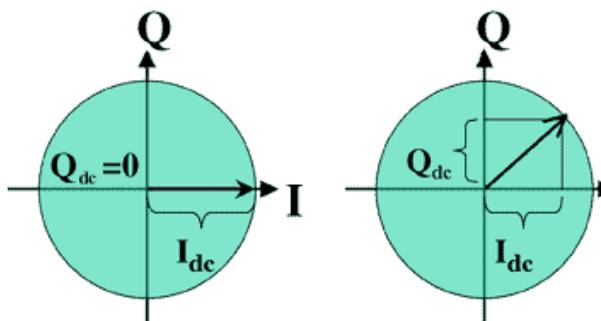
Multiplier Phase Detector – Simple but which signal is first?



I/Q DEMODULATOR



- Amplitude modulation: $s(t)= A(t)\sin(\omega t + \varphi)$
 $\sin(\alpha + \beta) = \cos(\alpha) \cos(\beta) - \sin(\alpha) \sin(\beta);$
- IQ Modulation: $s(t)= I(t)\cos(\omega t + \varphi(t))$ or $s(t)=I(t)\cos(\omega t) - Q(t)\sin(\omega t)$
where: $I(t)=A(t)\cos(\varphi(t))$ and $Q(t)= A(t)\sin(\varphi(t))$

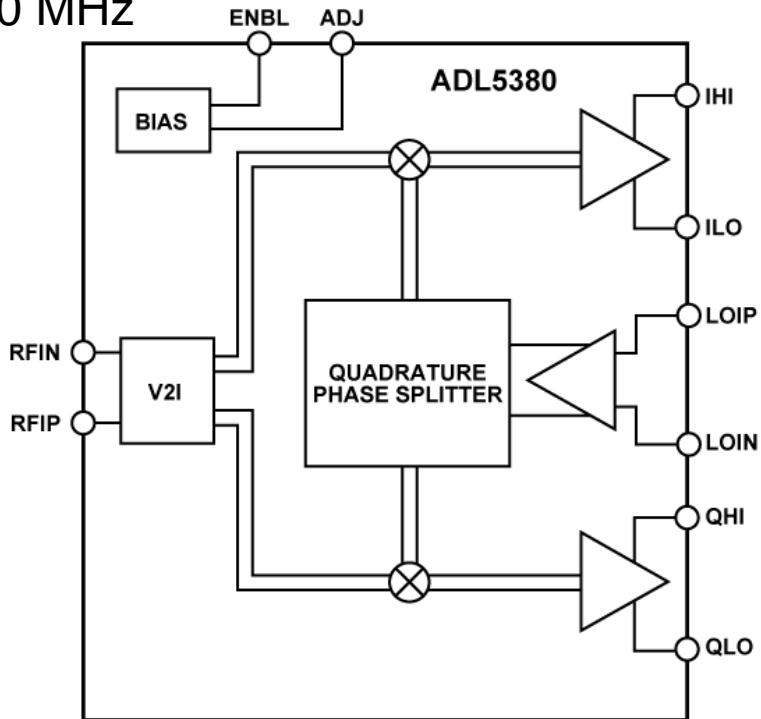


I/Q DEMODULATOR

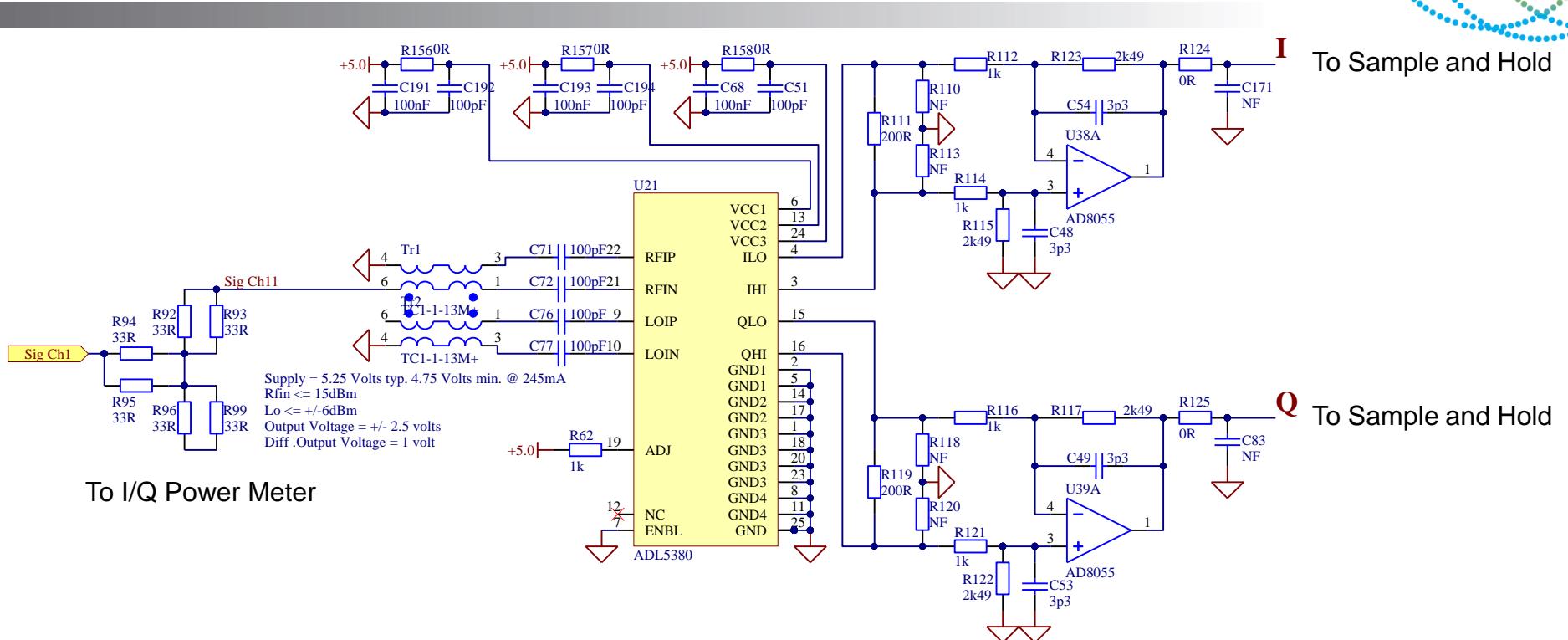


Key Features of ADL5380:

- Operating RF and LO frequency: 400 MHz to 6 GHz
- Input P1dB (IP1dB): 11.6 dBm @ 900 MHz
- Voltage conversion gain: ~7 dB
- Quadrature demodulation accuracy @ 900 MHz
- Phase accuracy: ~0.2°
- Amplitude balance: ~0.07 dB
- Demodulation bandwidth: ~390 MHz
- Baseband I/Q drive: 2 V p-p into 200 Ω
- Single 5 V supply

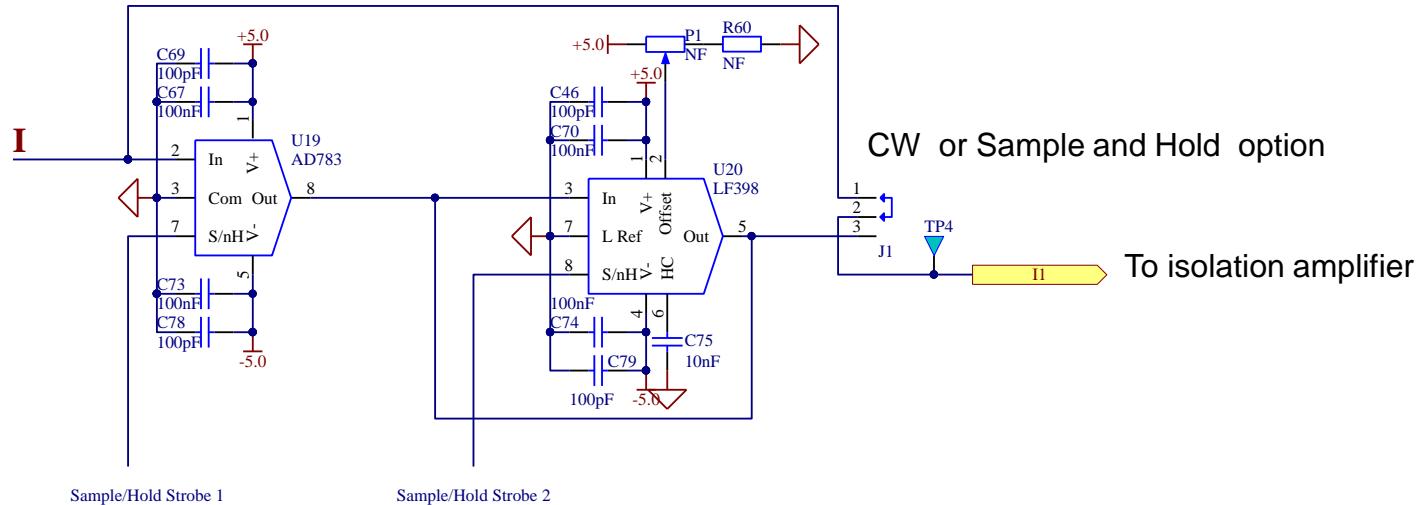


I/Q DEMODULATOR



- Differential amplifiers to extract I/Q signals and provide also filtering
- R124 and C171 additional low pass filter – if needed
- R110, R111 and R113 different options of loading outputs.

CW and Pulsed RF measurements - Sample and Hold



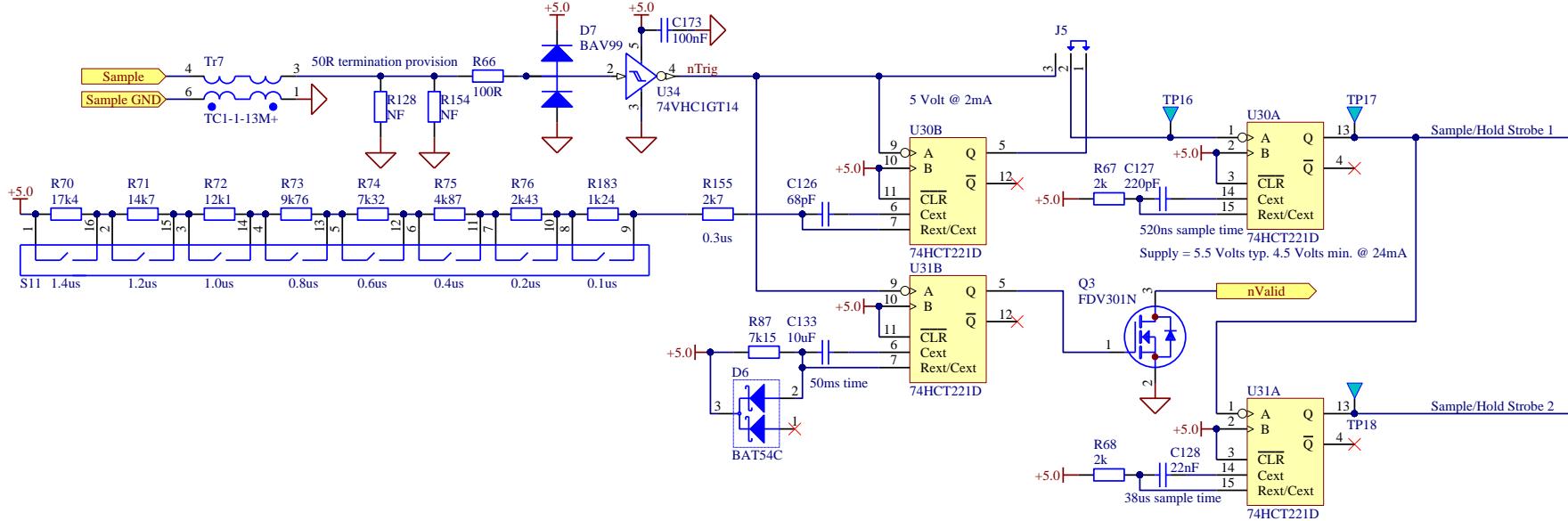
KFEATURES of AD783

- High speed Sample and Hold Amplifier
- Acquisition Time to 0.01%: 250 ns Typical
- Low Droop Rate: 0.02 mV/ms
- Fully Specified and Tested Hold Mode Distortion
- Internal Hold Capacitor

KFEATURES of LF398

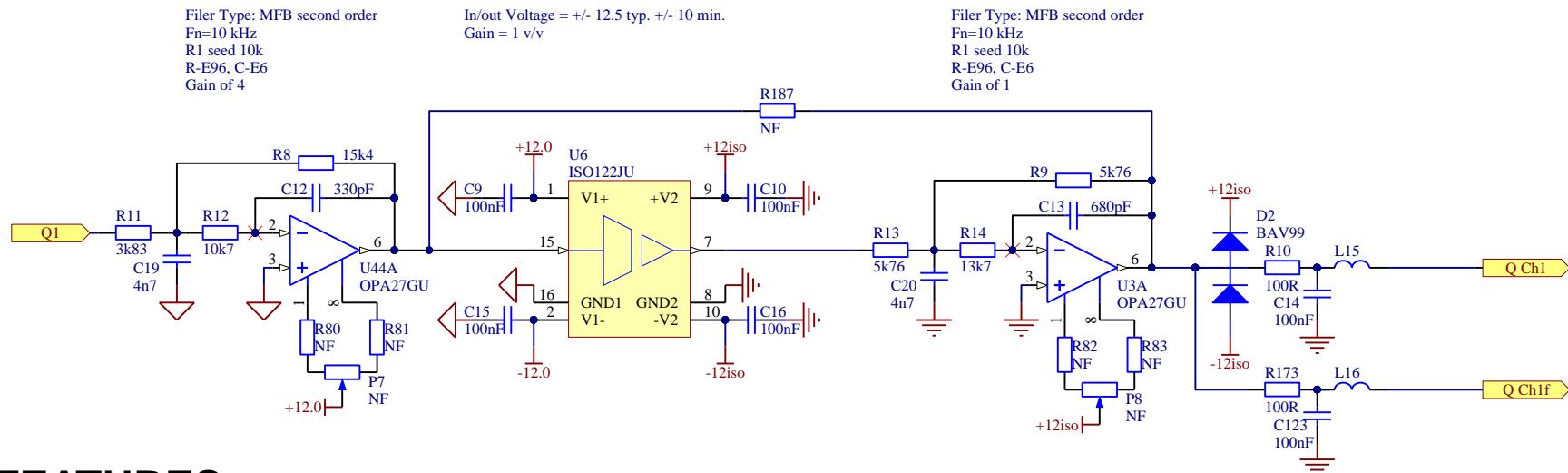
- Less than 10 μ s acquisition time
- 0.5 mV typical hold step at $C_h = 0.01 \mu F$
- Low input offset
- 0.002% gain accuracy
- High supply rejection ratio in sample or hold

CW and Pulsed RF measurements - Sample and Hold



- U30B - option to delay trigger signal
- Switch programmable delay
- Extended trigger pulse for visualisation purposes (Front Panel)
- Sub-sequential sample and hold triggers - U30A and U31A

OPTICAL ISOLATION AND FILTERING

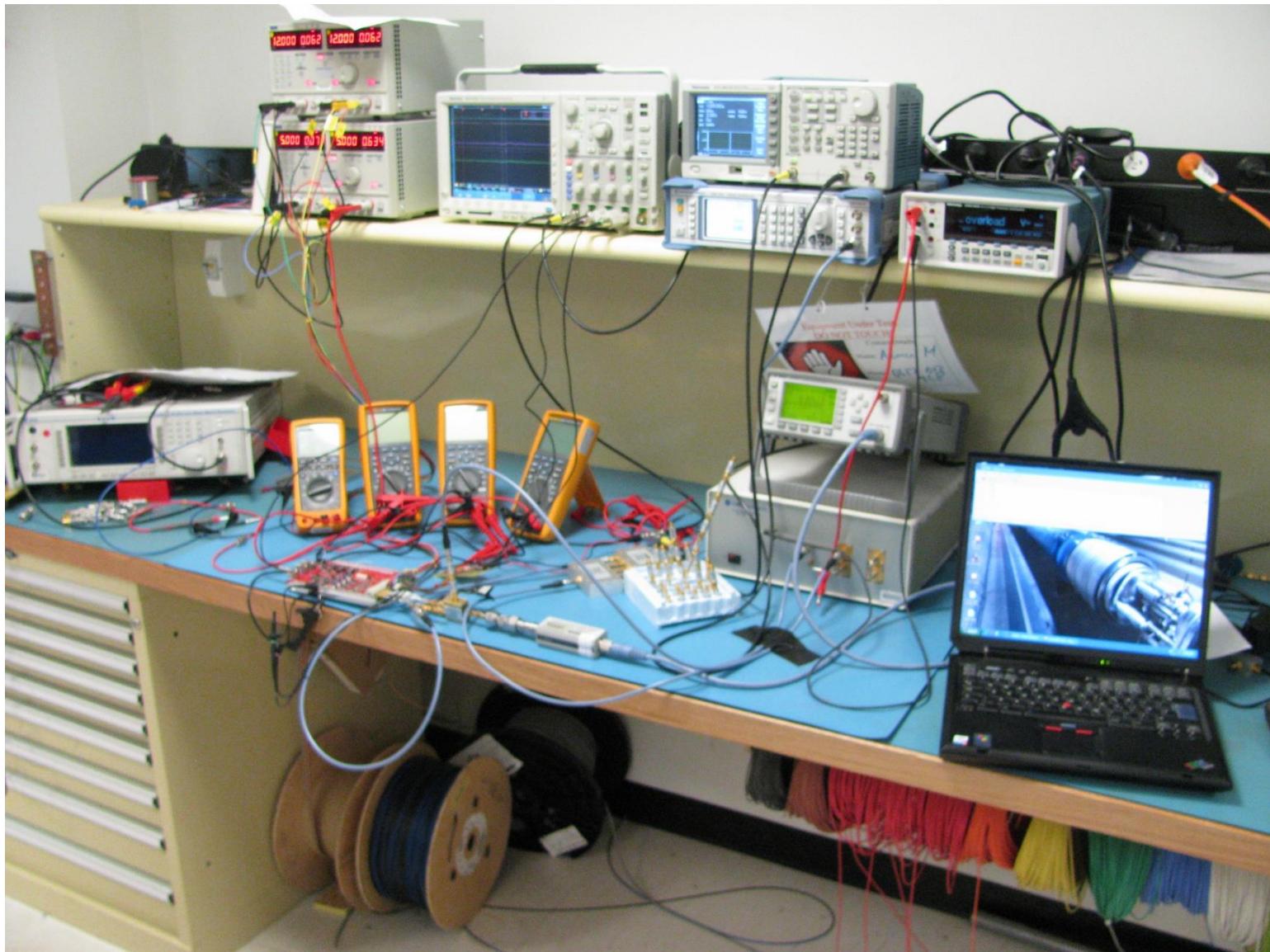


FEATURES

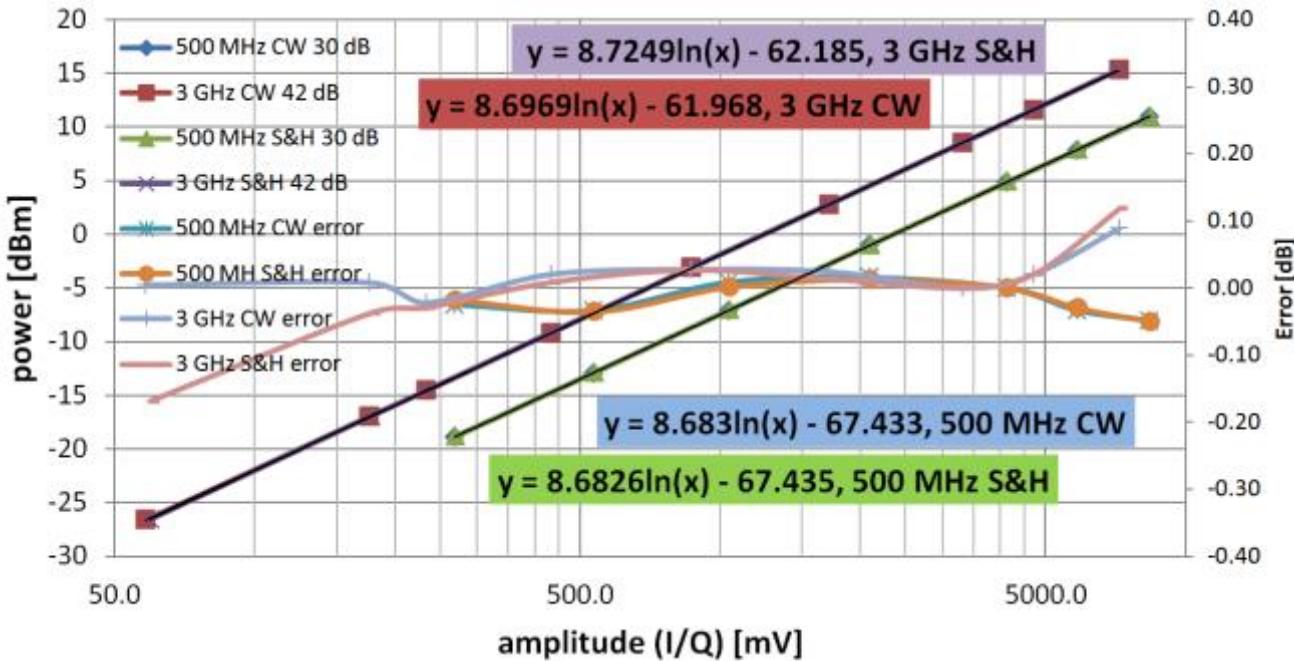
- 100% tested for high-voltage breakdown, rated 1500Vrms
- 0.010% max Nonlinearity
- Bipolar operation: $VO = \pm 10V$
- The signal is transmitted digitally across capacitive barrier – requires filtering!!!
- Again outputs and EMC protection components – never enough!

TESTING

2ns responds to 0.6m
0.1ps responds to 30um!



TESTING – Dynamic Range

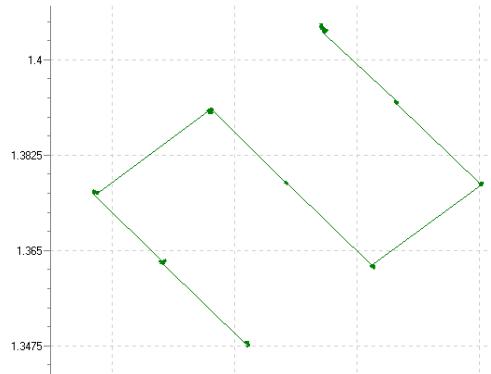


- The measured noise figures were excellent and achieved a resolution of 0.1 degrees and 0.02 dB respectively; and still remarkably 1 deg and 0.2 dB at -32 dB in pulsed mode.
- Both gains for CW and pulsed mode are equal without the need for adjustment.

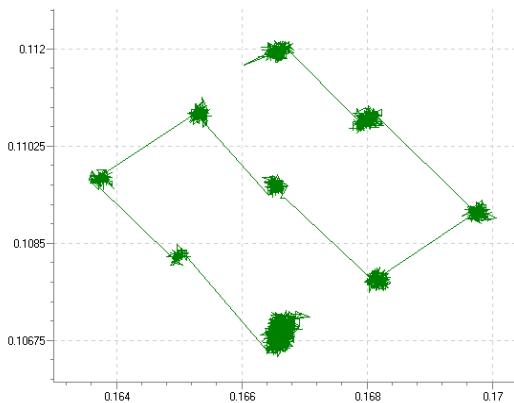
TESTING – Resolution



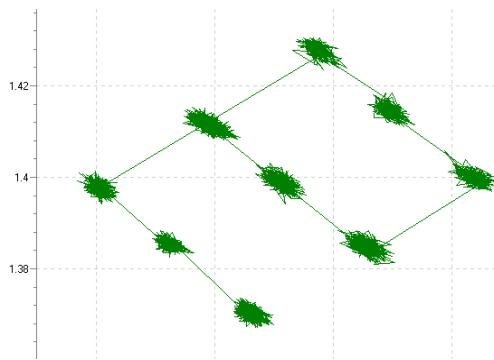
Input: 3 GHz, CW, 2.4 dBm
steps: 0.1 dB/0.5 ps (0.54 deg)
scale: 17.5 mV/div



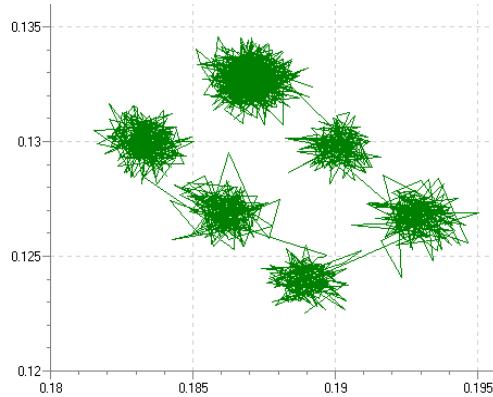
Input: 3 GHz, CW, -17dBm
steps: 0.1 dB/0.5 ps (0.54 deg)
scale: 1.75/2.00 mV/div



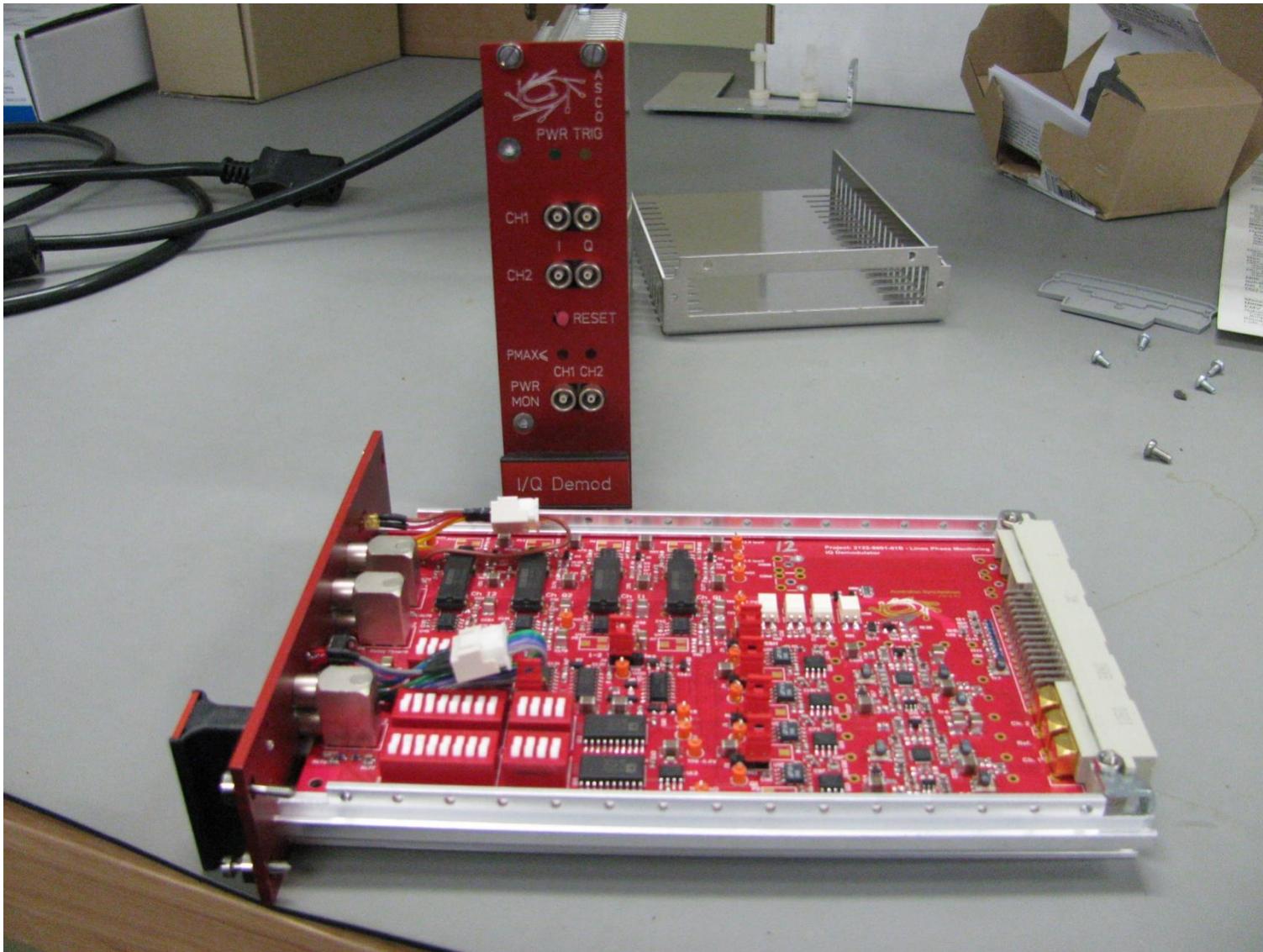
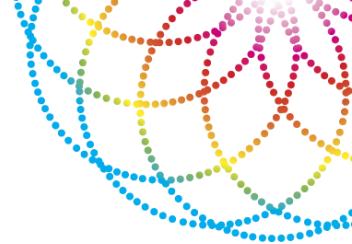
Input: 3 GHz, SH, 2.4 dBm
steps: 0.1dB 0.5ps (0.54 deg)
scale: 20 mV/div



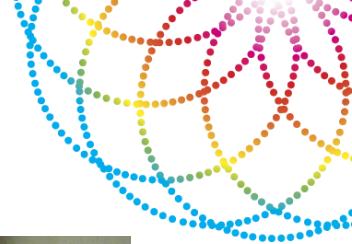
Input: 3 GHz SH -17dBm
steps: 0.2dB 1ps (1.08deg)
scale: 5 mV/div



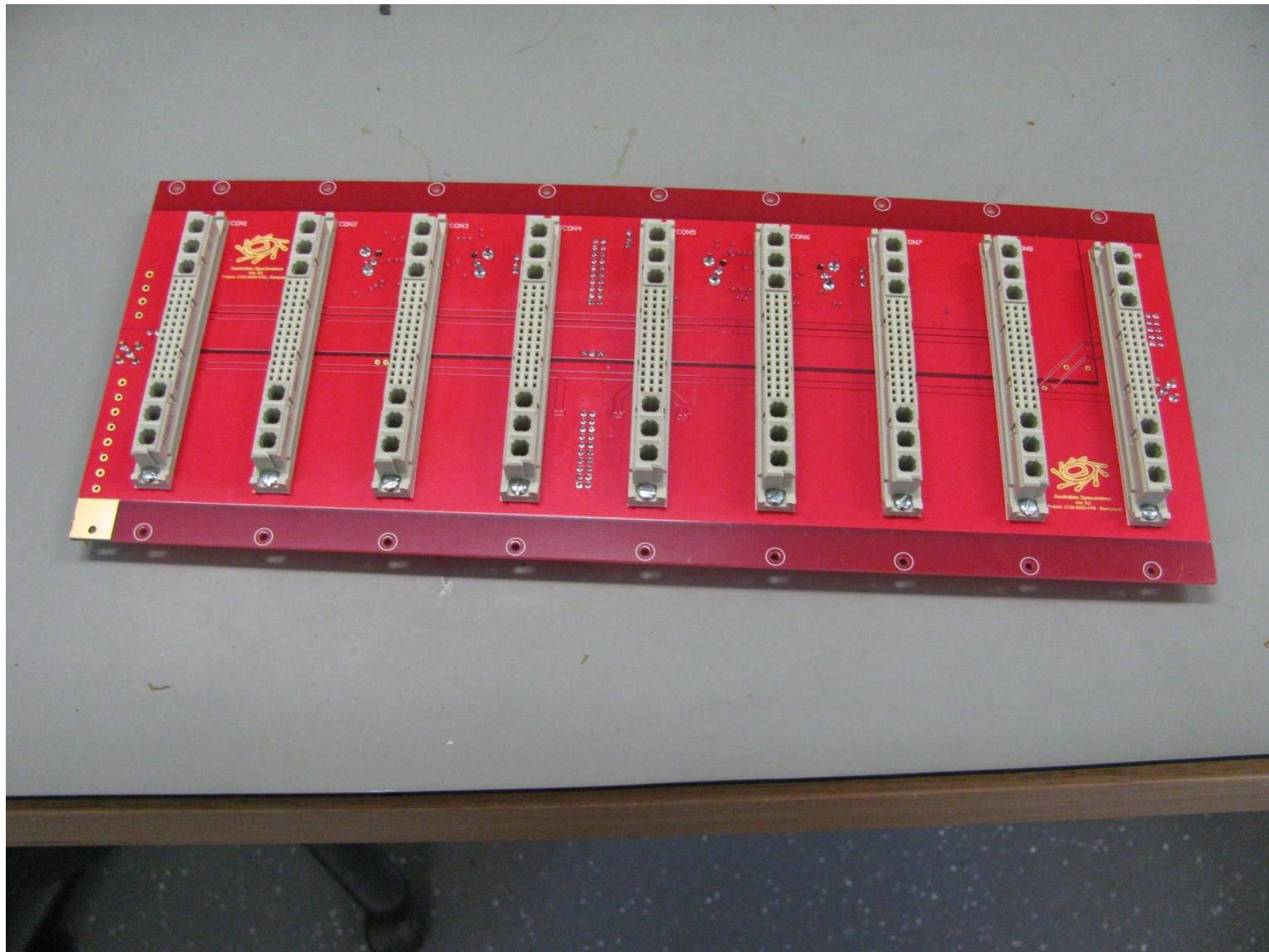
PACKAGING - 3U CRATE (boards 100x160)



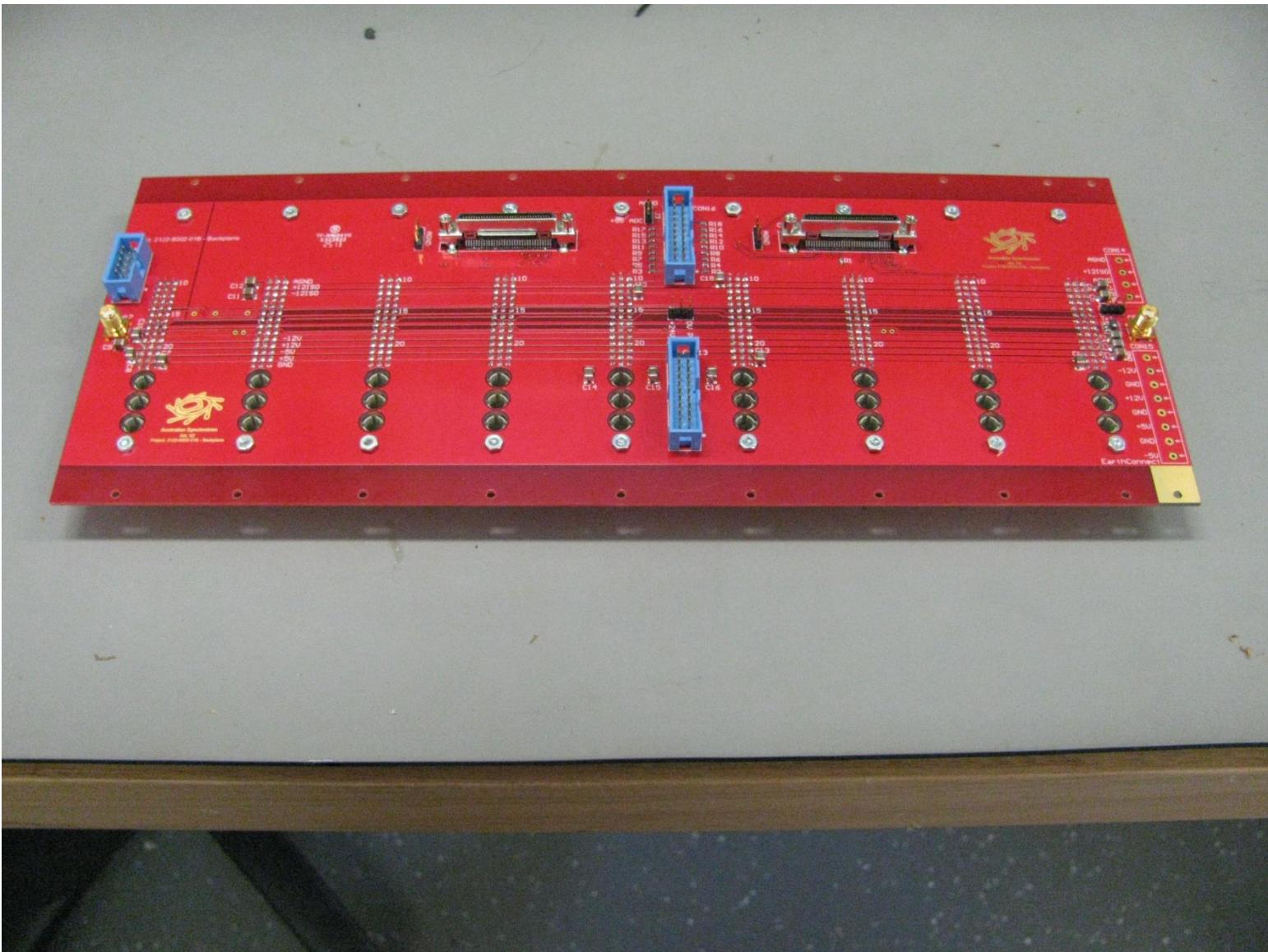
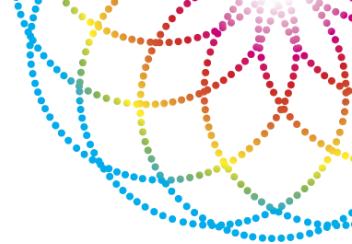
PACKAGING - 3U CRATE (boards 100x160)



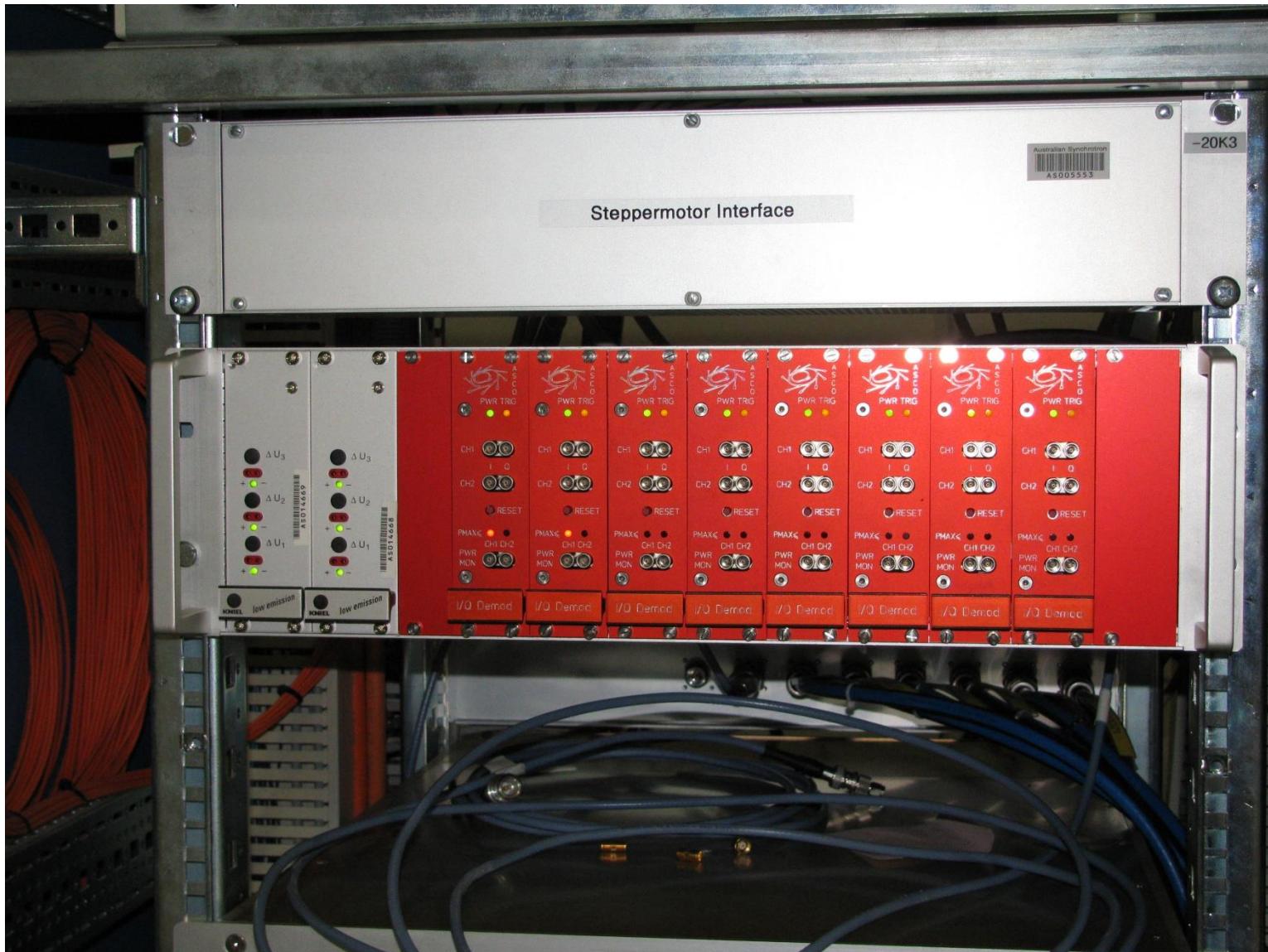
PACKAGING - 3U CRATE (Backplain)



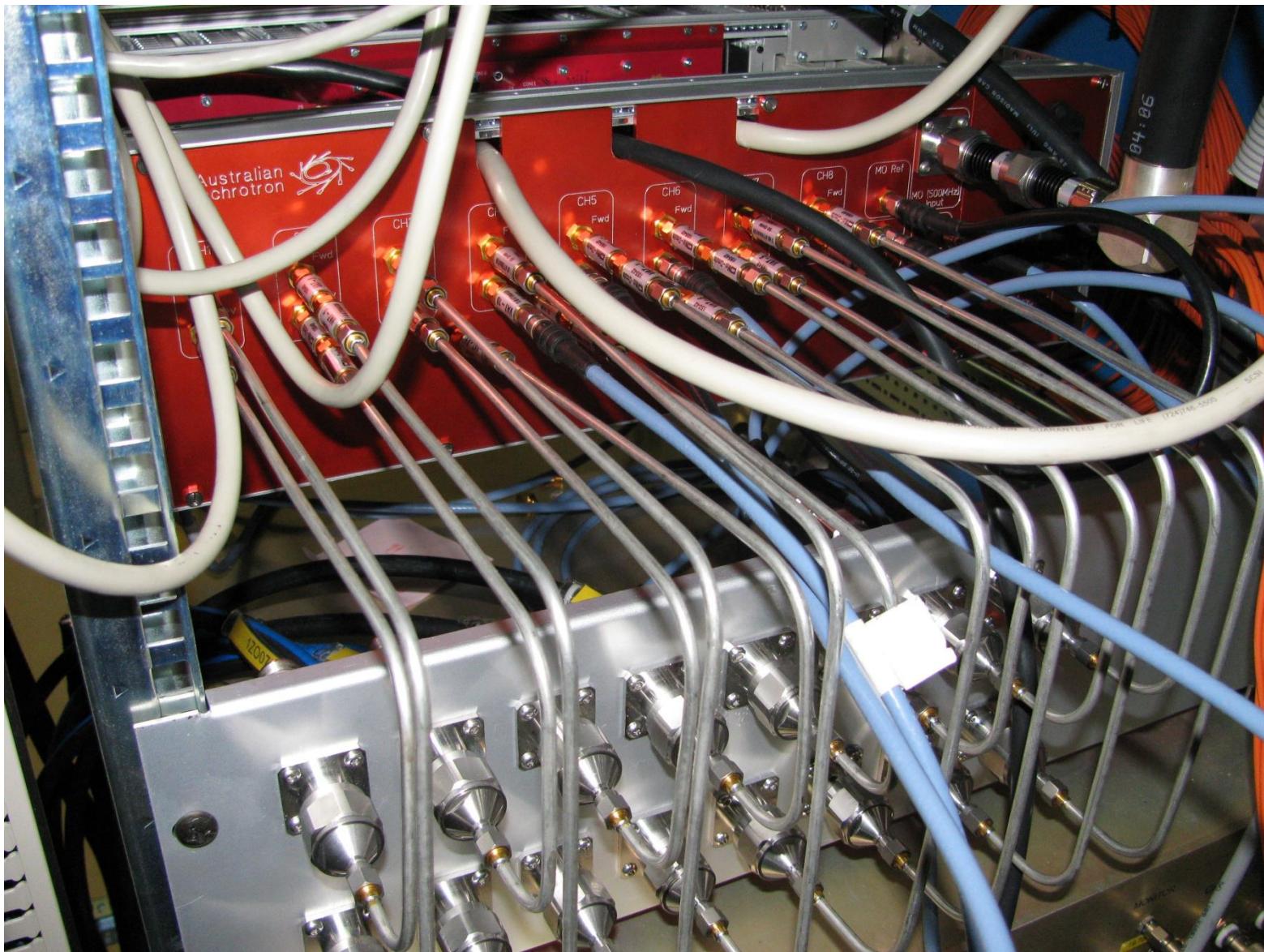
PACKAGING - 3U CRATE (boards100x160)



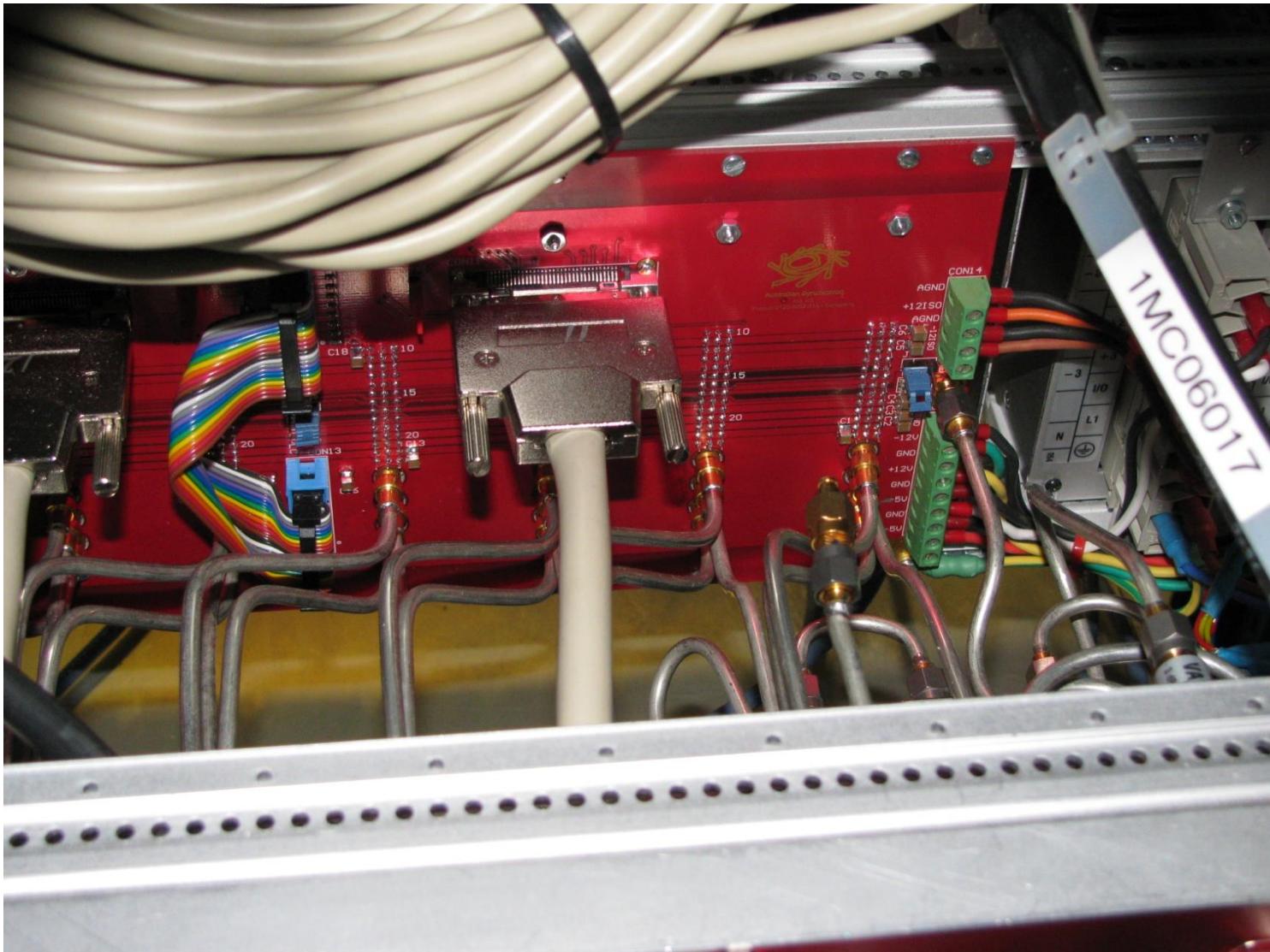
PACKAGING - 3U CRATE



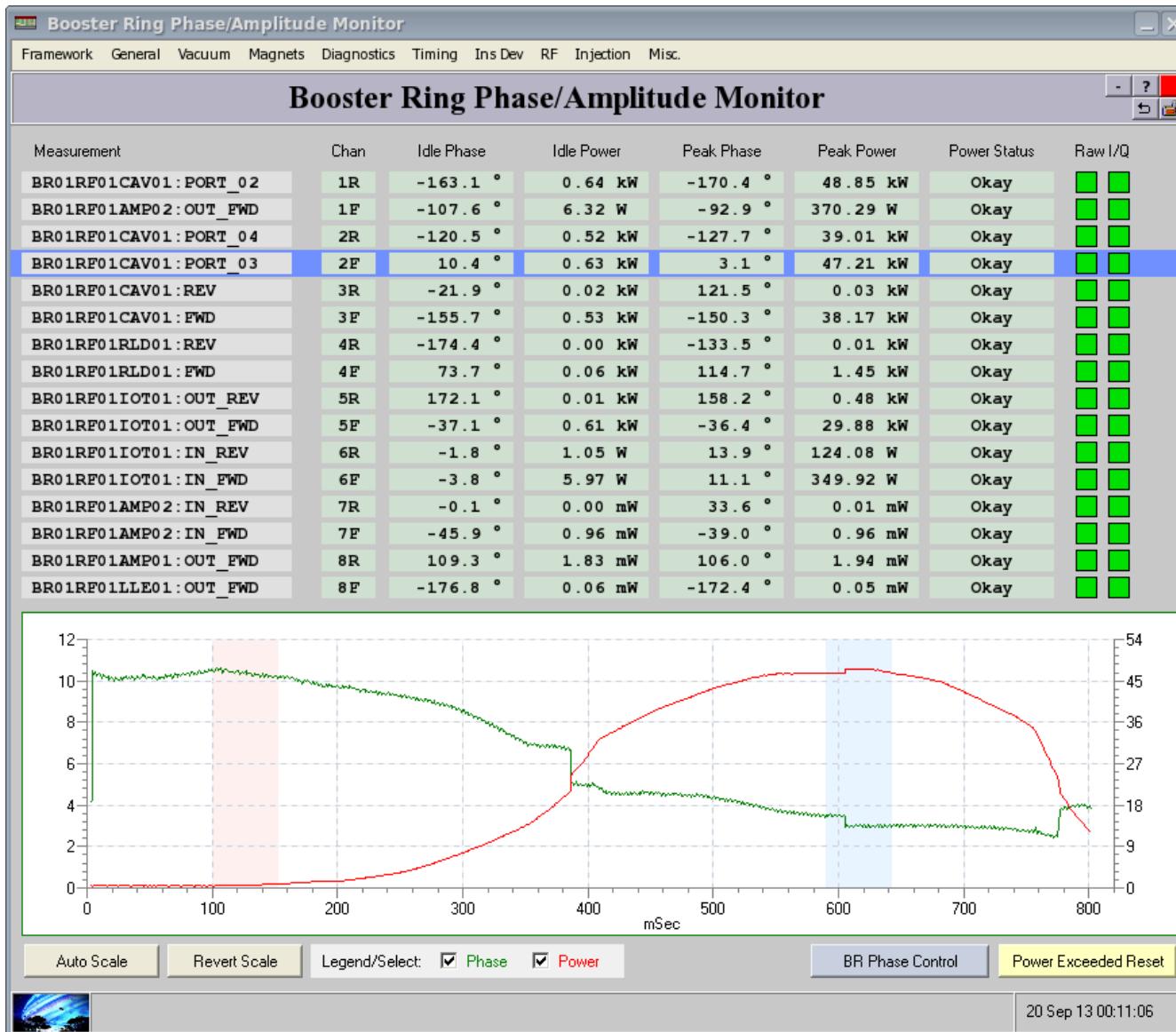
PACKAGING - 3U CRATE (Patch panel)



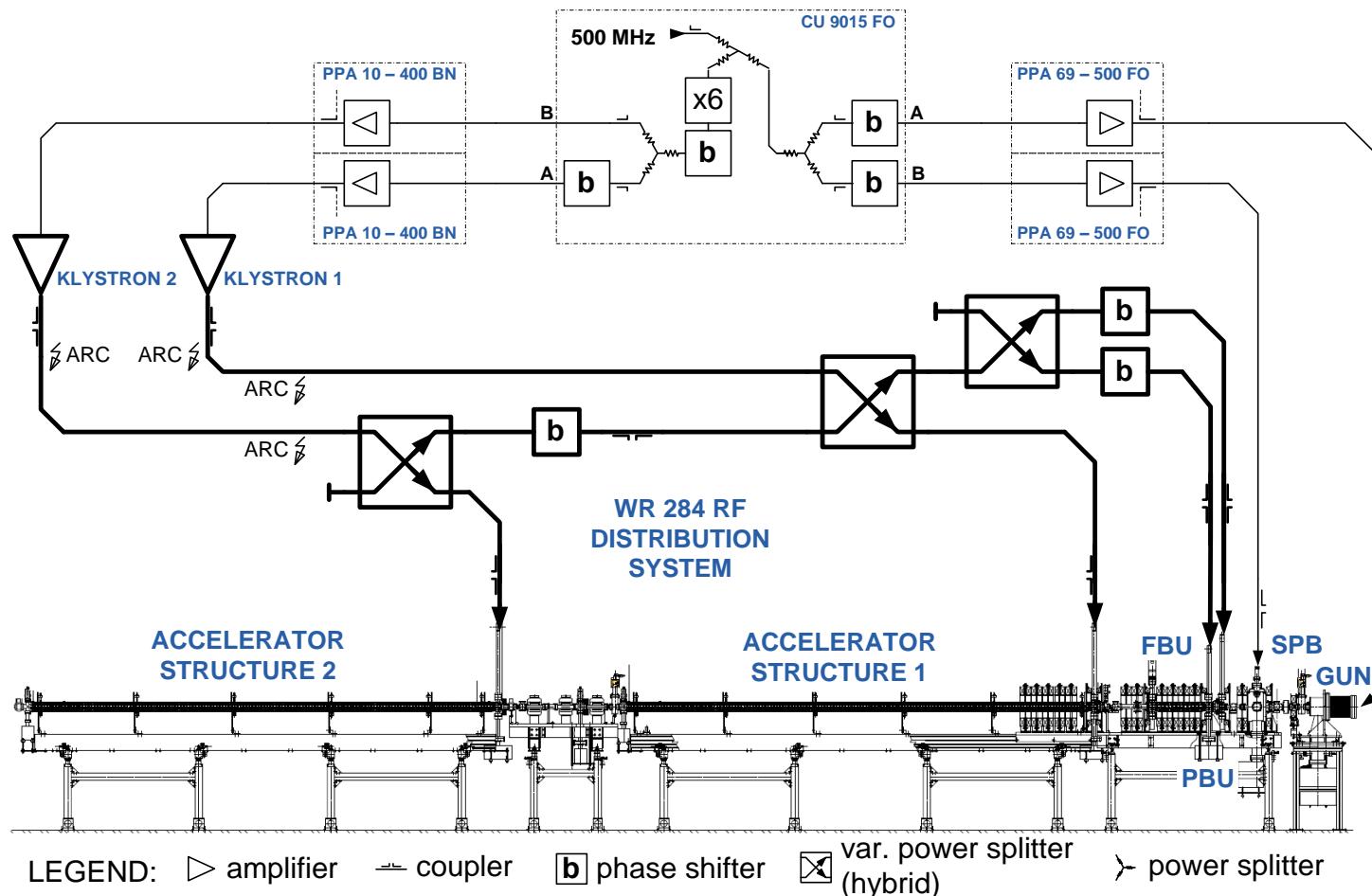
PACKAGING - 3U CRATE (Patch panel)



PRACTICAL APPLICATION AND OUTCOMES



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ACKNOWLEDGMENTS

K.L. Zingre,
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